II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (Previously Presented) A system for determining timing criticality information of an electrical circuit comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit;

wherein the timing criticality information is a node criticality probability of each of one or more nodes of the electrical circuit.

3. (Previously Presented) A system for determining timing criticality information of an electrical circuit comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit;

wherein the timing criticality information is a component criticality probability of each of one or more components of the electrical circuit.

4. (Previously Presented) A system for determining timing criticality information of an electrical circuit comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit;

wherein the timing criticality information is a path criticality probability of each of one or more paths of the electrical circuit.

5. (Previously Presented) The system as recited in claim 4, wherein the criticality probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

6. (Previously Presented) The system as recited in claim 4, wherein the criticality probability of a node of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that node.

7. (Previously Presented) The system as recited in claim 4, wherein the arrival tightness probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

8. (Previously Presented) The system as recited in claim 4, wherein the required arrival tightness probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

9. (Cancelled)

10. (Currently Amended) A ~~The~~ system for determining timing criticality information of an electrical circuit ~~as recited in claim 1~~ comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit, wherein the timing criticality information is used to determine a user-provided number of critical paths in order of criticality probability.

11. (Currently Amended) A ~~The~~ system for determining timing criticality information of an electrical circuit ~~as recited in claim 1~~ comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit, wherein the timing criticality information is used to determine one or more critical paths in order of criticality probability until the sum of the criticality probabilities exceeds a user-provided probability threshold.

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Previously Presented) A system for determining timing criticality information of an electrical circuit comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit;

wherein a separate rising and a separate falling criticality information is determined from the timing criticality information for each of the one or more nodes of the electrical circuit and for each of the one or more components of the electrical circuit.

17. (Cancelled)

18. (Previously Presented) A system for determining timing criticality information of an electrical circuit comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit;

wherein the electrical circuit is a sequential circuit that contains one or more of the following: an edge-triggered latch, a master-slave latch, a level-sensitive latch, and a transparent latch.

19. (Previously Presented) The system as recited in claim 18, wherein a guard time of a timing test is one of deterministic and statistical.

20. (Previously Presented) A system for determining timing criticality information of an electrical circuit comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit;

wherein the electrical circuit contains multiple clock phases.

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28. (Currently Amended) A ~~The~~ system for determining timing criticality information of an electrical circuit ~~as recited in claim 1~~ comprising:

a. a netlist input for receiving a circuit netlist, the circuit netlist representing a topology of the electrical circuit;

b. an assertion input for receiving one or more assertions representing boundary timing conditions;

c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;

d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for delay variation of each component of the electrical circuit, each model being a function of one or more of the sources of delay variation; and

e. a process that determines and outputs the timing criticality information of the electrical circuit, wherein a clock-edge information is one of deterministic and statistical.

29. (Previously Presented) A method for determining timing criticality information of an electrical circuit, comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting a statistical timing analysis of the electrical circuit;

d. storing an arrival tightness probability and a required arrival tightness probability at each of the one or more edges of the electrical circuit; and

e. determining a criticality probability of each of the one or more nodes of the timing graph and the one or more edges of the timing graph by a backward traversal of the timing graph.

30. (Previously Presented) A method for determining timing criticality information of an electrical circuit, comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting statistical timing analysis of the electrical circuit;

d. storing an arrival tightness probability and a required arrival tightness probability at each of the one or more edges of the electrical circuit;

e. determining an end point criticality probability of each of one or more end points of the timing graph; and

f. determining a criticality probability of the one or more nodes of the timing graph and the one or more edges of the timing graph by a backward traversal of the timing graph.

31. (Previously Presented) The method as recited in claims 29 and 30, wherein the timing criticality information is a path criticality probability of each of one or more paths of the electrical circuit.

32. (Previously Presented) The method as recited in claims 29 and 30, wherein the criticality probability of a component of the electrical circuit is used as an upper bound on a path criticality probability of any path of the electrical circuit including that component.

33. (Previously Presented) The method as recited in claims 29 and 30, wherein the criticality probability of a node of the electrical circuit is used as an upper bound on a path criticality probability of any path of the electrical circuit including that node.

34. (Previously Presented) The method as recited in claims 29 and 30, wherein the arrival tightness probability of a component of the electrical circuit is used as an upper bound on a path criticality probability of any path of the electrical circuit including that component.

35. (Previously Presented) The method as recited in claims 29 and 30, wherein the required arrival tightness probability of a component of the electrical circuit is used as an upper bound on a path criticality probability of any path of the electrical circuit including that component.

36. (Previously Presented) The method as recited in claims 29 and 30, wherein the timing criticality information is used to determine a path that has the highest probability of being critical.

37. (Previously Presented) The method as recited in claims 29 and 30, wherein the timing criticality information is used to determine a user-provided number of critical paths in order of criticality probability.

38. (Previously Presented) The method as recited in claims 29 and 30, wherein the timing

criticality information is used to determine a user-provided number of critical paths in order of criticality probability.

39. (Previously Presented) The method as recited in claims 29 and 30, wherein the timing criticality information is used to determine critical paths in order of criticality probability until the sum of the criticality probabilities exceeds a user-provided probability threshold.

40. (Previously Presented) The method as recited in claim 30, wherein the criticality probabilities are determined on the basis of the overall electrical circuit.

41. (Previously Presented) The method as recited in claim 29, wherein the criticality probabilities are determined on the basis of a single end point.

42. (Previously Presented) The method as recited in claims 29 and 30, wherein a late-mode criticality information is determined from the timing criticality information.

43. (Previously Presented) The method as recited in claims 29 and 30, wherein an early-mode criticality information is determined from the timing criticality information.

44. (Previously Presented) The method as recited in claims 29 and 30, wherein separate rising and falling criticality information is determined for each of the one or more nodes of the timing graph and for each of the one or more edges of the timing graph.

45. (Previously Presented) The method as recited in claims 29 and 30, wherein the electrical circuit is one or more of the following:

combinational circuit, a sequential circuit, a static logic circuit, and a dynamic logic circuit.

46. (Previously Presented) The method as recited in claims 29 and 30, wherein the electrical circuit is a sequential circuit that contains one or more of the following: an edge-triggered latch, a master-slave latch, a level-sensitive latch, and a transparent latch.

47. (Previously Presented) The method as recited in claims 29 and 30, wherein a guard time of a timing test is one of deterministic and statistical.

48. (Previously Presented) The method as recited in claims 29 and 30, wherein the electrical circuit contains multiple clock phases.

49. (Previously Presented) The method as recited in claims 29 and 30, wherein the parameterized delay model for each component of the electrical circuit comprises one or more of: a deterministic part, a correlated part, and an independently random part.

50. (Previously Presented) The method as recited in claims 29 and 30, wherein the sources of variation are correlated.

51. (Previously Presented) The method as recited in claims 29 and 30, wherein the sources of variation are independent.

52. (Previously Presented) The method as recited in claims 29 and 30, wherein the parameterized delay models are prestored in a table.

53. (Previously Presented) The method as recited in claims 29 and 30, wherein the parameterized delay models are prestored as coefficients of delay equations.

54. (Previously Presented) The method as recited in claims 29 and 30, wherein the parameterized delay models are determined by circuit simulation on-the-fly.

55. (Previously Presented) The method as recited in claims 29 and 30, wherein each of the one or more assertions is one of deterministic and statistical.

56. (Previously Presented) The method as recited in claims 29 and 30, wherein a clock-edge information is one of deterministic and statistical.

57. (Previously Presented) A system for determining timing criticality information of an electrical circuit, comprising:

a. means for reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. means for building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. means for conducting a statistical timing analysis of the electrical circuit;

d. means for storing an arrival tightness probability and a required arrival tightness probability at each of the one or more edges of the electrical circuit; and

e. means for determining the criticality probability of each of the one or more nodes of the timing graph and the one or more edges of the timing graph by a backward traversal of the timing graph.

58. (Previously Presented) A system for determining timing criticality information of an electrical circuit, comprising:

a. means for reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. means for building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. means for conducting statistical timing analysis of the electrical circuit;

d. means for storing an arrival tightness probability and a required arrival tightness probability at each of the one or more edges of the electrical circuit;

e. means for determining an end point criticality probability of each of one or more end points of the timing graph; and

f. means for determining a criticality probability of each of the one or more nodes of the timing graph and the one or more edges of the timing graph by a backward traversal of the timing graph.

59. (Previously Presented) A memory storage device storing a method for determining timing criticality information of an electrical circuit, the method comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting a statistical timing analysis of the electrical circuit;

d. storing an arrival tightness probability and a required arrival tightness probability at each of the one or more edges of the electrical circuit; and

e. determining a criticality timing probability of each of the one or more nodes of the timing graph and the one or more edges of the timing graph by a backward traversal of the timing graph.

60. (Previously Presented) A memory storage device storing a method for determining timing criticality information of an electrical circuit, the method comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting statistical timing analysis of the electrical circuit;

d. storing an arrival tightness probability and a required arrival tightness probability at each of the one or more edges of the electrical circuit;

e. determining an end point criticality probability of each of ~~the~~ one or more end points of the timing graph; and

f. determining a criticality probability of each of the one or more nodes of the timing graph and the one or more edges of the timing graph by a backward traversal of the timing graph.

61. (Previously Presented) An output product produced by a process for determining timing criticality information of an electrical circuit, the process comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting a statistical timing analysis of the electrical circuit;

d. storing an arrival tightness probability and a required arrival tightness probabilities at each of the one or more edges of the electrical circuit; and

e. determining a criticality probability of each of the one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal

62. (Previously Presented) An output product produced by a process for determining timing criticality information of an electrical circuit, the process comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting statistical timing analysis of the electrical circuit;

d. storing an arrival tightness probability and a required arrival tightness probability at each of the one or more edges of the electrical circuit;

e. determining an end point criticality probability of each of one or more end points of the timing graph; and

f. determining a criticality probability of each of the one or more nodes of the timing graph and the one or more edges of the timing graph by a backward traversal of the timing graph.